ABSTRACT OF THE DISCLOSURE

A low density parity check (LDPC) code that is particularly well adapted for hardware implementation of a belief propagation decoder circuit (38) is disclosed. The LDPC code is arranged as a parity check matrix (***H***) whose rows and columns represent check sums and input nodes, respectively. The parity check matrix is grouped into subsets of check sum rows, in which the column weight is a maximum of one. The decoder circuitry includes a parity check value estimate memory (52). Adders (54) generate extrinsic estimates, from immediately updated input node probability estimates, and the extrinsic estimates are applied to parity check update circuitry (56) for generating new parity check sum value estimates. These parity check sum value estimates are stored back into the memory (52), and after addition with the extrinsic estimates, are stored in a column sum memory (66) of a corresponding bit update circuit (60) as updated probability values for the input nodes.